ANT-20, ANT-20E
Advanced Network Tester

PDH MUX/DEMUX

BN 3035/90.30 to 90.31

Drop & Insert

BN 3035/90.20
in combination with
PDH MUX/DEMUX

Software Version 7.20

Operating Manual

4

BN 3035/98.23

WAVETEK
WANDEL
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Communications Test Solutions

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Contents

Introduction

Options BN 3035/90.30 to BN 3035/90.32

1 Multiplex and demultiplex functions

The ANT-20 can generate and analyze PDH frames with complete channel structures at rates of 2, 8, 34 and 140 Mbit/s when fitted with the PDH Multiplexer/Demultiplexer Chain option. This allows testing of the multiplex functions of individual hierarchy levels right up to tests covering all hierarchies from 140 Mbit/s down to 64 kbit/s including linking to SDH signals via the appropriate mapping stages.

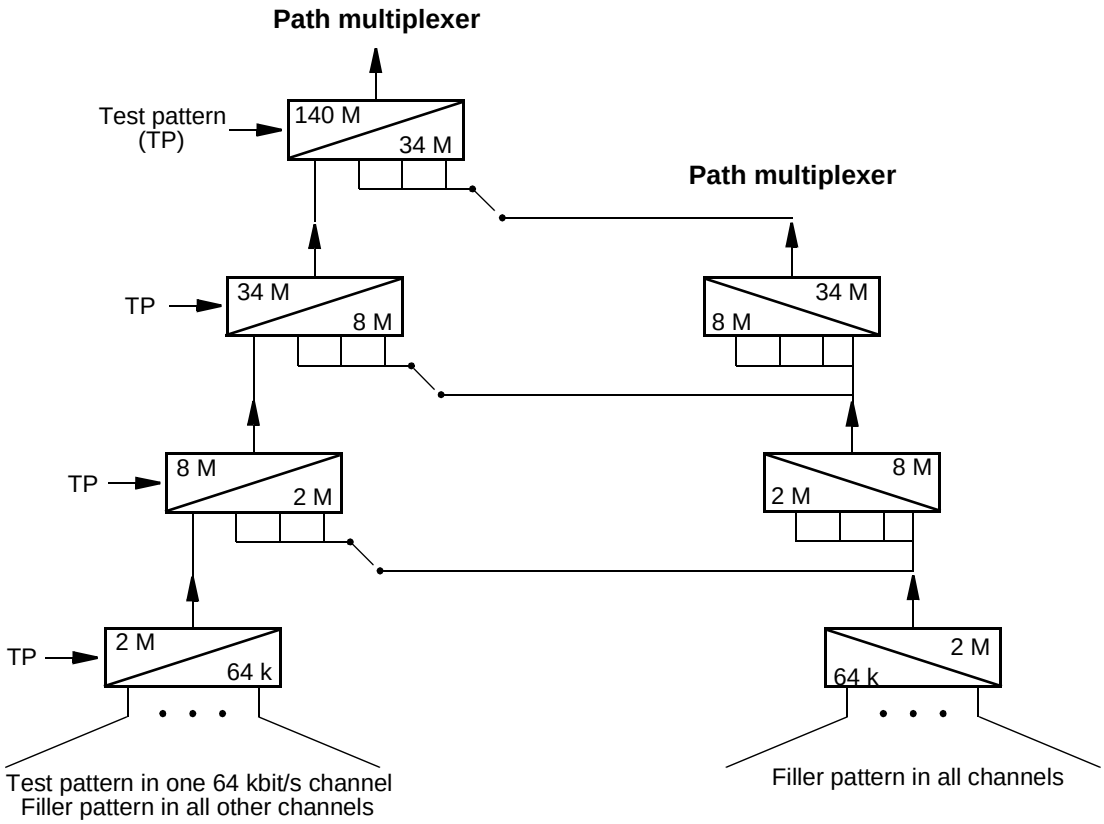

Fig. I-1 TX signal structure

2 Testing switch and sensor functions

Switch functions

SDH and PDH network elements process the PDH signals of various hierarchy levels. Complex, interleaved signal paths occur, particularly in modern SDH network nodes (cross-connects). The linking of the PDH multiplex chain to the SDH mapping functions in the ANT-20 makes the instrument ideal for testing complex switching functions. Since the ANT-20 can generate and evaluate structured signals right down to the 64 kbit/s level, it can test switching functions on all hierarchy levels from 140 Mbit/s to 64 kbit/s. Tests can be performed between two SDH ports or between an SDH and a PDH port.

Alarm sensor test

Comprehensive facilities for inserting errors into the PDH signal at various hierarchy levels allow testing of the monitor functions built in to the network elements. This is particularly useful during installation work, as the network management systems are dependent on the correct functioning of these sensors during subsequent operation.

3 In-service monitoring of tributary channels

The demultiplex function provides access to the tributary channels right down to the 64 kbit/s level. This permits pinpoint in-service monitoring of individual channels in PDH signals and in SDH signals when the appropriate mappings are employed.

Specifications

Options BN 3035/90.30 to BN 3035/90.32

1 Generator section

1.1 Frame generator, 64k/140M PDH MUX/DEMUX Chain (option BN 3035/90.30)

The following frames are available:

Bit ratekbit/s	Frame conforming to:	Notes
2048	ITU-T G.704	PCM 30, PCM 30 CRC, PCM 31 and PCM 31 CRC systems
8448	ITU-T G.742	PCM 120 system
34368	ITU-T G.751	PCM 480 system
139264	ITU-T G.751	PCM 1920 system

Table S-1 Frame generation

The multiplexer chain (BN 3035/90.30) allows generation of a completely structured signal from 64 kbit/s to 140 Mbit/s.

1.2 Frame alignment signals

Frame alignment signals (FAS) corresponding to ITU-T recommendations G.751, G.742 and G.704.

1.2.1 Frame bit modifications

The following bits can be statically programmed:

PCM 1920 (G.751) . . . . . FAS bit nos. 13, 14, 15, 16

PCM 480, 120 (G.751, G.742) . . . . . FAS bit nos. 11, 12

PCM 30/31 (G.704) . . . . . NFAS bit nos. 3 through 8

PCM 30/31 CRC (G.704) . . . . . NFAS bit nos. 3 through 8

The following bits can be dynamically programmed:

PCM 30/ PCM 30 CRC (G.704). . . . . NFAS bit nos. 4 through 8 (S_a4 through S_a8)

Bits S_a4 thruogh S_a8 can be selected and each loaded with a freely programmable pattern 8 bits in length. This permits transmission of S_a sequences.

For PCM 30 / PCM 30 CRC systems, frame 0 or 1 in timeslot 16 can be loaded with a freely programmable 8 bit word. Frames 2 through 15 can be loaded with a further freely programmable 8 bit word.

1.2.2 CRC checksum (PCM 30 CRC / PCM 31 CRC)

The ANT-20 calculates the CRC checksum for the measured channel and the filler channels as per ITU-T recommendation G.704 and inserts the result bits at the appropriate position in the pulse frame.

1.3 Justification as per ITU-T G.742 and G.751

The bit rates in the upper and subordinate systems are in a fixed relationship to each other.

Justification is at a nominal rate (offset of upper and subordinate systems is identical). Exception: Insertion of external signals.

Upper system bit rate in kbit/s	ITU-T	Justification ratio	Nominal justification rate in kbit/s
8448	G.742	0.42424	4.226
34368	G.751	0.43575	9.750
139264	G.751	0.41912	9.934

Table S-2 Justification

1.3.1 PDH tributary offset

Static offset for the PDH tributary bit rates during insertion into the SDH container.

Offset . . . . . ±100 ppm
for all bit rates, relative to SDH container
Step width . . . . . 1 ppm

The offset is an average value. The actual offset at any given time may be above or below this value.

1.4 Error insertion (anomalies)

In addition to the error types described in the “Specifications” for the mainframe instrument, the following anomalies can be inserted:

Error type, anomaly[1]	Single	Rate[2]
CRC-4	yes	2E-3 to 1E-8
E bit	yes	2E-3 to 1E-8

1 For PCM 30 CRC and PCM 31 CRC only
2 A CRC word error rate is inserted

Table S-3 Available error types (anomalies) in addition to the mainframe instrument

The insertion of **errors** (anomalies) **or alarms** (defects) are mutually exclusive. The action selected first is active.

1.5 Alarm generation (defects)

The alarm types are described in the “Specifications” for the mainframe instrument.

The insertion of **alarms** (defects) **or errors** (anomalies) are mutually exclusive. The action selected first is active.

1.6 Test signals for bit error rate measurements

1.6.1 Internal test signals

Bit patterns as in the mainframe instrument:

- Transmitted in all timeslots (framed pattern to ITU-T O.150/O.151)
- Transmitted in a selected timeslot

1.6.2 External signal (with option 3035/90.20 only)

An external signal with bit rate 34 368 kbit/s (coaxial), 8 448 kbit/s (coaxial) or 2 048 kbit/s (coaxial or balanced) can be inserted into the selected timeslot instead of the bit pattern (see Sec. 1.6.1).

The interfaces for this signal are described in the “Specifications” for the STM-1 mapping options.

1.6.3 Filler signals

Complete structured signals using the pseudo-random bit sequence PRBS 6 are transmitted in all timeslots except the selected timeslot in all 64 kbit/s channels.

2 Receiver section

2.1 Frame systems

Frames which can be evaluated by the 64k/140M PDH MUX/DEMUX chain and 64k/140M PDH DEMUX chain (options BN 3035/90.30 and 3035/90.31)

Bit rate kbit/s	Frame conforming to	Notes
2048	ITU-T G.704	PCM 30, PCM 31 systems
2048	ITU-T G.704/G.706	PCM 30 CRC, PCM 31 CRC systems
8448	ITU-T G.742	PCM 120 system
34368	ITU-T G.751	PCM 480 system
139264	ITU-T G.751	PCM 1920 system

Table S-4 Frame systems for individual system bit rates

All timeslots can be selected for all PCM frame structures. These may be speech or data channels in a primary rate system or the tributary channels in a justified multiplex system.

2.2 Evaluation

2.2.1 Frame bit evaluation

The following bits are evaluated and displayed:

PCM 1920 (G.751) . . . . . FAS bit nos. 13, 14, 15, 16

PCM 480, 120 (G.751, G.742). . . . . FAS bit nos. 11, 12

PCM 30/31 (G.7049) . . . . . NFAS bit nos. 1 through 8

PCM 30/31 CRC (G.704). . . . . NFAS bit nos. 2 through 8 (A bit, S_a4 through S_a8)

For PCM30/31 CRC systems, one of the bits S_a4 through S_a8 can be selected in order to display pattern sequences of up to 8 bits in length.

The D alarm bits (RDI alarms) are also evaluated and indicated by means of LEDs.
Also see in the ”Specifications” of the mainframe instrument.

2.2.2 CRC evaluations (PCM 30 CRC / PCM 31 CRC)

Errored CRC words are evaluated in the selected channel (CRC word error count).

The equivalent CRC bit error ratio is calculated from the CRC word error ratio.

The number of E bit errors is also converted to the equivalent bit error ratio.

2.3 Offset measurements

All offsets in the hierarchy stages in the measurement path are measured simultaneously and displayed.

Display in ppm

2.4 Error measurements (anomalies)

The error measurements are described in the “Specifications” for the mainframe instrument. The frame alignment signals in all hierarchy stages of the selected path are checked simultaneously.

2.5 Alarm detection (defects)

The detected alarms are described in the “Specifications” for the mainframe instrument. The RDI alarms in all hierarchy stages of the selected path are checked simultaneously.

2.6 Evaluation of test signals for bit error measurements

2.6.1 Internal evaluation

Evaluation:

- in all timeslots (framed pattern to ITU-T O.150/O.151)
- in the selected timeslot

2.6.2 External signal (with option 3035/90.20 only)

Output of a signal with bit rate 34 368 kbit/s (coaxial), 8 448 kbit/s (coaxial) or 2 048 kbit/s (coaxial or balanced) for external evaluation is alternative or simultaneous with internal evaluation (see Sec. 2.6.1).

The interfaces for this are described in the “Specifications” for the “STM-1 mapping” options.

3 Drop&Insert / Through Mode / Block&Replace

Option: BN 3035/90.20

3.1 Functions

This Option provides the following functions for all PDH multiplex options fitted to the ANT-20.

Drop&Insert

Generator and receiver operate independently as mapper and demapper. The signal from a selected channel is dropped from the receive signal and output to a connector. An external signal is inserted into the transmit signal.

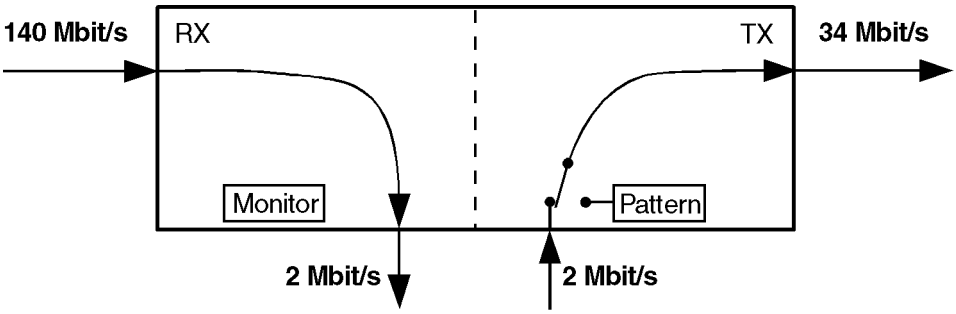

Fig. S-1 Drop&Insert: Generator and receiver operate independently

An unbalanced digital input and output are provided on the mainframe instrument for dropping and for inserting tributary signals (see Sec. 3.2.1, Page S-8 and Sec. 3.3.1, Page S-9).

The mainframe instrument is also equipped with a balanced output [13] and input [12] for dropping and for inserting tributary signals via balanced interfaces.

Through Mode

The received signal is looped through the ANT-20 and re-transmitted by the generator.

The ANT-20 operates in Through Mode as a signal monitor without affecting the signal.

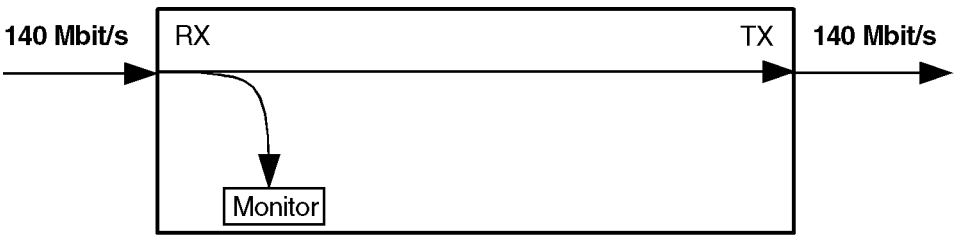

Fig. S-2 Through Mode: Generator and receiver coupled

The looped-through signal can also be jittered using the Jitter Generator options (Jitter Generator up to 155 or 622 Mbit/s, BN 3035/90.60 to 61). This function is available for all bit rates fitted to the instrument.

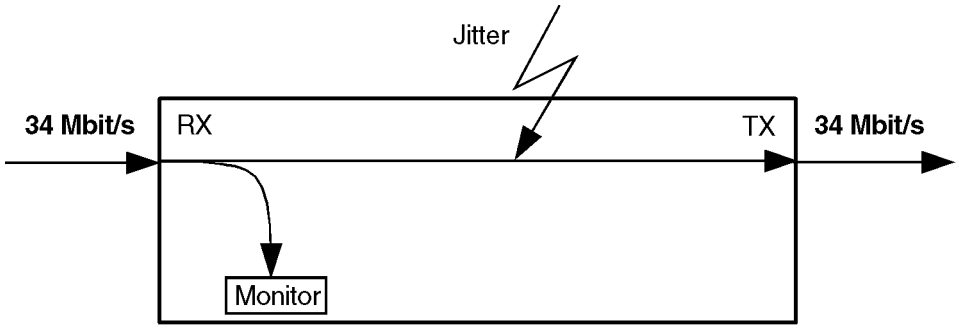

Fig. S-3 Through Mode: Adding jitter to the looped-through signal

Block&Replace

In PDH mode not possible.

3.1.1 Clock generator

Drop&Insert

As specified in the “Specifications” of the mainframe instrument.

Through Mode

In Through Mode, clock generation is always derived from the receive signal clock. No signal offset is possible in this operating mode (see also the “Specifications” of the mainframe instrument).

3.1.2 Anomaly insertion

Drop&Insert

As specified in Sec. 1.4, Page S-3.

Through Mode

Anomaly insertion is not possible.

3.1.3 Defect generation

Drop&Insert

As specified in Sec. 1.5, Page S-3.

Through Mode

Defect generation is not possible.

3.1.4 Measurements

There are no restrictions on measurements (see Sec. 2, Page S-4).

3.2 Signal outputs

3.2.1 AUXILIARY signal output [11], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Output impedance . . . . . 75 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E4	139.264	CMI	± 0.5 V
DS3	44.736	B3ZS	± 1.0 V
E3	34.368	HDB3	
E2	8.448	HDB3	± 2.37 V
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-5 Specifications of the AUXILIARY signal output [11], electrical

3.2.2 LINE/AUXILIARY signal output [13], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Output impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted peak spurious input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Output voltage
E1	2.048	HDB3	± 3.0 V
DS1	1.544	B8ZS	DSX-1 compatible
The bit rates depend on the mapping options fitted.			

Table S-6 Specifications of the LINE/AUXILIARY signal output [13], electrical

The balanced output is used as a LINE or as an AUXILIARY output.

3.3 Signal inputs

3.3.1 AUXILIARY signal input [10], electrical

Connector . . . . . unbalanced, (coaxial)

Socket type . . . . . BNC

Input impedance . . . . . 75 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Input voltage range . . . . . 0 dB attenuation referred to nominal level

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E4	139.264	CMI	1.0 V ±10 %
DS3	44.736	B3ZS	1.0 V ±10 %
E3	34.368	HDB3	
E2	8.448	HDB3	2.37 V ±10 %
E1	2.048	HDB3	
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-7 Specifications of the AUXILIARY signal input [10], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

3.3.2 LINE/AUXILIARY signal input [12], electrical

Connector . . . . . balanced

Socket type . . . . . Lemo SA (Bantam)

Input impedance
2.048 Mbit/s . . . . . 120 Ω
1.544 Mbit/s . . . . . 100 Ω

Max. permitted frequency offset . . . . . ± 500 ppm

Max. number of consecutive zeros for line code = AMI 15

Max. permitted peak input voltage . . . . . ± 5 V

Interface	Bit rate (Mbit/s)	Line code	Input voltage
E1	2.048	HDB3	3.0 V ±10 %
DS1	1.544	B8ZS	
The bit rates depend on the mapping options fitted.			

Table S-8 Specifications of the LINE/AUXILIARY signal input [12], electrical

LOS (Loss of Signal) status display

LED lights up if the signal input is active but no signal is present.

The balanced input is used as a LINE or as an AUXILIARY input.